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Bulletin Date:	5/23/2012		Bulletin Effective Date:	5/23/2012
Title:	Si114x enhances 1.8V IO tolerance; datasheet update			
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<div align="center">Bulletin Details</div>

Description:

Silicon Labs is pleased to announce the enhancement of the Si114x product to support 1.8V IO and Vdd rails. New test limits will permit +/-5% margin around the 1.8V Vdd level (1.71V min) to conform to 1.8V voltage rails and IO. No application hardware or software changes are required as a result of this enhancement.

In addition the pin description for pin 5 has been clarified as a Do Not Connect (DNC) from the previously labeled No Connect (NC).

The ordering part number remains the same: Si114x-A11-GMR. The silicon, package, footprint, and pin out remain unchanged. The corresponding datasheet is Si114x Rev 1.3 and is available now. Please refer to the document change list in the datasheet for details on these updates and other minor clarifications.

Reason:

The new test limits enable margin around the 1.8V Vdd operating level, thereby allowing functionality for systems using 1.8V IO.

Product Identification:

This bulletin applies to all members of the Si114x product family, including those shown below. The ordering part numbers are not changing:

- Si1141-A11-GMR
- Si1142-A11-GMR
- Si1143-A11-GMR

Devices with the new 1.8V Vdd and IO specification will be shipping from Silicon Labs starting May 28, 2012. After this date, all devices shipped will conform to this specification.

Customer Actions Needed:

None